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Appellants Brief
7-15-03

ATTORNEY DOCKET NO. - S. LYTLE 18 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Stephen A. Lytle

Serial No.: 09/667,046

Filed: September 21, 2000

For: DUAL DAMASCENE PROCESS
WITH NO PASSING METAL FEATURES

Group: 2811

Examiner: Hung K. Vu

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop Appeal Brief-Patents

CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this correspondence, including the attachments listed, is being deposited as First Class Mail with the United States Postal Service, in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313, on the date shown below.

June 27, 2003 Stephanie Pritt
Date of Mailing Signature of person mailing

ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated January 28, 2003, of Claims 21, 24, 25, 29, and 30. The Appellant submits this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $ 320.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner

to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF INVENTION

VI. ISSUES

VII. GROUPING OF CLAIMS

VIII. PRIOR ART

IX. APPELLANTS' ARGUMENTS

X. APPENDIX A - CLAIMS

XI. APPENDIX B - FIGURE 8

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems, Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 21, 24, 25, 29, and 30 are pending. Claims 1-20, 22-23, and 26-28 were withdrawn or canceled during prosecution. Claims 21, 24, 25, 29, and 30 currently stand rejected and no claims are objected to or allowed. Claims 21, 24, 25, 29, and 30 are being appealed.

IV. STATUS OF THE AMENDMENTS

The present Application was filed on September 21, 2000 wherein Claims 1-28 were submitted. On September 18, 2002, an election of claims was filed withdrawing Claims 1-20 without traverse. In response to an Examiner's Action mailed December 5, 2001, the Appellant filed a first Amendment on March 11, 2002. A Request for Continued Examination together with a Preliminary Amendment canceling Claims 22, 23, and 26 was filed on July 22, 2002. In response to a July 31, 2002, Office Action, a second Amendment was filed on November 6, 2002 adding Claims 29-30 . A Final Rejection on was mailed on January 28,2002 and the Appellant filed a third Amendment canceling Claims 27-28 on March 24, 2003. In an Advisory Action mailed April 1,

2003, the Examiner entered the amendments but stated that the Application was not in condition for allowance. The Appellant then filed a Notice of Appeal.

V. SUMMARY OF THE INVENTION

Among other things, this invention is directed, in general, to a semiconductor device where a via between second and third interlevel dielectric layers does not have a landing pad. In an exemplary embodiment, a first interconnect metal is located on or in a first interlevel dielectric layer and a second interconnect metal is located on or in a second interlevel dielectric layer where the second interlevel dielectric layer is located over the first interlevel dielectric layer. A third interconnect metal is then located on or in a third interlevel dielectric layer where the third interlevel dielectric layer is located over the second dielectric layer. The device has a via located through the second and third interlevel dielectric layers, connecting the first and third interconnect metals, which via does not have a landing pad between the second and third interlevel dielectric layers. Attached as APPENDIX B is FIGURE 8 of the present Application, illustrating one embodiment of the invention.

VI. ISSUES

A. First Issue Presented for Review:

Whether Claims 21, 24 and 25, as rejected by the Examiner, are anticipated by U.S. Patent No. 6,127,260 to Huang and, therefore, are unpatentable under 35 U.S.C. §102(e).

B. Second Issue Presented for Review:

Whether Claims 21, 24 and 25, as rejected by the Examiner, are anticipated by U.S. Patent No. 6,177,340 to Yoo, *et al.* ("Yoo") and, therefore, are unpatentable under 35 U.S.C. §102(e).

C. Third Issue Presented for Review:

Whether Claims 29 and 30, as rejected by the Examiner, are anticipated by U.S. Patent No. 6,163,067 to Inohara, *et al.* ("Inohara") and, therefore, are unpatentable under 35 U.S.C. §102(e).

VII. GROUPING OF THE CLAIMS

Claims 21, 24 and 25 form a first group of claims and Claims 29 and 30 form a second group.

VIII. PRIOR ART

A. Huang

Huang describes a process for forming a narrow diameter opening in thick insulator layers. The process allows the aspect ratio for a narrow diameter opening to be reduced by utilizing a two stage opening procedure. A first stage is used to create a first narrow diameter opening, in composite insulator layers, via an anisotropic RIE procedure. An isotropic wet etch procedure is then employed to widen the first narrow diameter opening in an overlying, doped silicon oxide component of the composite insulator layers, while the openings in the underlying, undoped silicon oxide components of the composite insulator layers do not increase in diameter. This tee shaped opening is used to accommodate a tee shaped metal structure that features a wide metal shape, which is located in the widened opening in the doped silicon oxide component of the composite insulator

layers. A second narrow diameter opening is then formed in an overlying, planarized insulator layer, exposing a portion of the top surface of the wide metal shape of the tee shaped metal structure. Formation of an upper metal plug in the second narrow diameter opening concludes the process of forming a metal structure in a narrow diameter opening, reducing the aspect ratio of the narrow diameter opening via a two stage opening procedure.

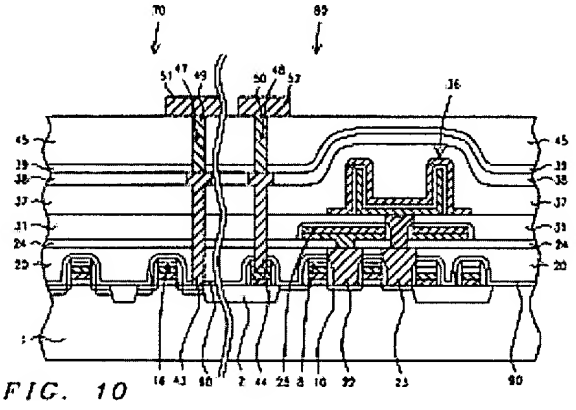


FIG. 10

Illustration 1

B. Yoo

Yoo describes a method for reducing the high aspect ratios, encountered when forming and filling narrow diameter contact holes in thick insulator layers. Yoo features a two step contact hole opening and filling procedure. First, lower narrow diameter contact holes are opened in lower levels of insulator layers and filled with tungsten. After deposition of upper levels of insulator layers, the upper narrow diameter contact holes are formed, exposing the tungsten filled, lower diameter contact holes. A second tungsten layer fills the upper, narrow diameter contact hole, resulting in a final

narrow diameter contact hole, in thick insulator layers, formed with reduced aspect ratios. These are formed via use of two contact hole openings and two tungsten fill procedures. These procedures also allow a damascene, tungsten bit line structure, to be formed in a dual shaped opening in lower insulator layers.

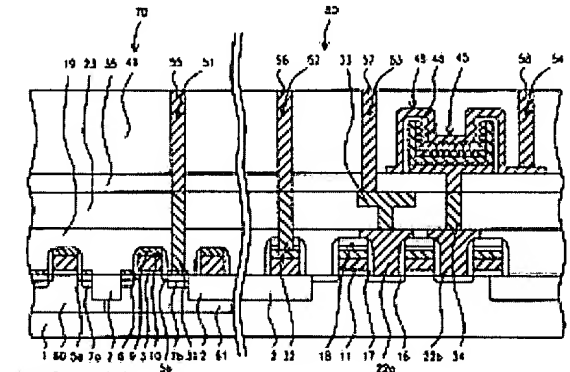


FIG. 20

Illustration 2

C. Inohara

Inohara describes a semiconductor apparatus and a process for fabricating the same that permits a reduction in the width of a wiring pattern of the semiconductor apparatus and the distance between wiring elements. Inohara describes using a stopper film and an insulating film on a substrate. A pattern of the contact hole is formed in the stopper film and a wiring pattern is formed on the resist film. The insulating films are etched by RIE with the resist film and stopper film used as masks. The etching rate of RIE for the insulating film is greater than that for the stopper film. Thus, a groove for formation of wiring and a contact hole for formation of a contact plug are simultaneously formed in a self-alignment manner.

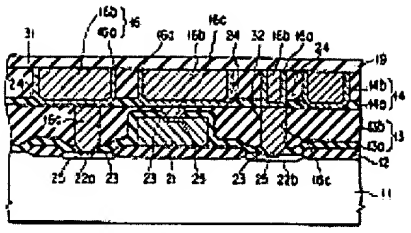


FIG. 13

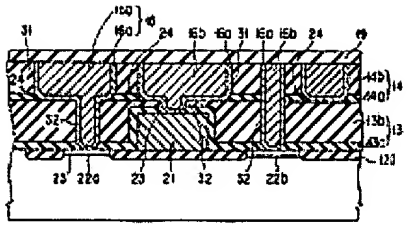


FIG. 14

Illustration 3

IX. THE APPELLANTS' ARGUMENTS

The inventions set forth in independent Claims 21 and 29 and their respective dependent claims are not anticipated by the references on which the Examiner relies. These references and the reasons they do not anticipate Appellants invention are hereinafter set forth:

A. Rejection of Claims 21, 24 and 25 as anticipated by Huang.

The Examiner rejected Claims 21, 24 and 25 under 35 U.S.C. §102 (e) as being anticipated by Huang. The Examiner asserts that the metal silicide 13 disclosed in Huang reads on the first interconnect metal recited in Claim 21. However, the metal silicide 13 disclosed in Huang is not an interconnect metal. Those skilled in the art understand that interconnects are layers of conductive metal that electrically couple various integrated components and circuits of a device. In fact, the ordinary definition of an "interconnect" feature requires that the feature couple or otherwise connect two other features - it must be the connection between the other features. The metal silicide 13 in

Huang does not interconnect other components or circuits. In direct contrast, the metal silicide 13 is one of the various components or features that is interconnected by an interconnect (comprising an interconnect metal structure 52), as shown in FIG. 10. Thus, the metal silicide 13 is interconnected by an interconnect metal, but the metal silicide 13 is not itself an interconnect metal.

The Examiner also asserts that the tee-shaped, lower metal plug structure 44 disclosed in Huang reads on the second interconnect metal recited in Claim 21. However, the lower metal plug structure 44 is a via, not an interconnect metal. As those skilled in the art understand, and as used in the present application, vias are metal filled openings between various layers of a semiconductor device that provide electrical connection between the layers. (Page 2, lines 7-10). The lower metal plug structure 44, in conjunction with the upper metal plug structure 50, clearly provides such electrical connection through various insulative layers (20, 24, 31, 38, 39 and 45) and between the overlying interconnect metal structure 52 and the underlying metal silicide 13. (FIG. 10). Thus, the lower metal plug structure 44 is a via, not an interconnect. Moreover, the Examiner asserts that the narrow opening 42a is a via (as discussed below), yet maintains that the lower metal plug structure 44 is an interconnect, even though the lower metal plug structure 44 is formed in the narrow opening 42a. Those skilled in the art understand that interconnect structures are not formed in vias. Accordingly, the lower metal plug structure 44 does not read on the second interconnect metal recited in Claim 21.

The Examiner also asserts that the narrow opening 42a disclosed in Huang reads on the via recited in Claim 21 of the present application. However, as discussed above, a via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers. In contrast, the narrow opening 42a is merely an empty opening, and does not

provide electrical connection between layers in the absence of the metal plug structure 44 subsequently formed therein. Therefore, the narrow opening 42a disclosed in Huang is not a via as recited in Claim 21.

Huang does not disclose each and every element of the claimed invention and, as such, fails to anticipate independent Claim 21 and dependent Claims 24 and 25. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 21, 24 and 25 as anticipated by Huang.

B. Rejection of Claims 21, 24 and 25 as anticipated by Yoo.

The Examiner rejected Claims 21, 24 and 25 under 35 U.S.C. §102(e) as being anticipated by Yoo. The Examiner takes the position that the titanium silicide layer 9 reads on the first interconnect metal recited in Claim 21. However, as discussed above with respect to Huang, a silicide layer comprising a portion of a gate structure is not an interconnect. Moreover, Yoo fails to disclose that the titanium silicide layer 9 is interconnected to any other component. For example, as shown in FIG. 20, the titanium silicide layer 9 remains isolated between a polysilicon layer 4, silicon nitride spacers 6 and a silicon oxide insulator layer 19. (See also, FIGs. 3 and 6). Thus, not only is the titanium silicide layer 9 not an interconnect metal, but the titanium silicide layer 9 is not even interconnected to other components by actual interconnect structure.

The Examiner also asserted that the tungsten plug 31 disclosed in Yoo reads on the second interconnect metal recited in Claim 21 of the present application. As also discussed above with respect to Huang, the tungsten plug 31 is a via and not an interconnect metal. More specifically, the lower tungsten plug 31 (in conjunction with the upper tungsten plug 55) clearly provides electrical

connection through various insulative layers (19, 23, 35 and 49) to a source/drain region 5a/5b. (See FIGs. 1 and 20). As such, the lower tungsten plug 31 is a via. Moreover, the Examiner asserted that the contact hole opening 27 is a via (as discussed below), yet maintains that the tungsten plug 31 is an interconnect, even though the tungsten plug 31 is formed in the contact hole opening 27. Again, those skilled in the art understand that interconnect structures are not formed in vias. Thus, the tungsten plug 31 does not read on the second interconnect metal recited in Claim 21.

The Examiner also asserted that the upper tungsten plug 55 disclosed in Yoo reads on the third interconnect metal recited in Claim 21 of the present application. However, in the same manner as discussed above regarding the lower tungsten plug 31, the upper tungsten plug is a via, not an interconnect. The upper tungsten plug 55 (in conjunction with the lower tungsten plug 31) provides electrical connection through various insulative layers (19, 23, 35 and 49) to a source/drain region 5a/5b. (See FIGs. 1 and 20), which is a function of a via and not of an interconnect.

The Examiner also asserted that the contact hole openings 27 and 51 disclosed in Yoo read on the via recited in Claim 21 of the present application. However, as discussed above with respect to Huang, a via is a metal filled opening between various layers of a semiconductor device that provides electrical connection between the layers. In contrast, the contact hole openings 27 and 51 are merely openings, and do not provide electrical connection between layers in the absence of the tungsten plugs 31 and 55 subsequently formed therein. Therefore, the contact hole openings 27 and 51 disclosed in Yoo do not read on the via recited in Claim 21.

Yoo fails to disclose each and every element recited in Claim 21 of the present application and, therefore, fails to anticipate Claim 21 and its dependent Claims 24 and 25. Accordingly, the

Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claims 21, 24 and 25 as anticipated by Yoo.

C. Rejection of Claims 29 and 30 as anticipated by Inohara.

The Examiner asserted that the silicide layer 25 disclosed in Inohara reads on the first metal feature recited in Claim 29. However, the silicide layer 25 is not located on a semiconductor surface, as is the first metal feature recited in Claim 29. In contrast, the silicide layer 25 is located in source/drain regions 22a/22b. Therefore, the silicide layer 25 does not read on a first metal feature located on a semiconductor surface, as recited in Claim 29.

The Examiner also asserted that the stopper film 13a disclosed in Inohara reads on the first etch stop layer recited in Claim 29 of the application. However, the stopper film 13a is not located on the silicide layer 25. In contrast, the stopper film 13a is located over and laterally adjacent the silicide layer 25. In fact, Inohara discloses using the stopper film 13a as a mask to form the underlying silicide layer 25, such that edges of openings in stopper film 13a coincide with the outer edges of the silicide layer 25. (Column 9, lines 52-65; column 11, lines 15-24). Accordingly, the silicide layer 25 lies only within an opening in the stopper film 13a, such that the stopper film 13a is not located on the silicide layer 25. Therefore, the stopper film 13a does not read on a first etch stop layer located on a first metal feature, as recited in Claim 29.

The Examiner also asserted that the contact hole 32 reads on the unsegmented via recited in Claim 29. However, as discussed above with respect to Huang and Yoo, a contact hole is not a via. Again, a via is a metal filled opening between various layers of a semiconductor device that provides

electrical connection between the layers. Thus, an empty, un-filled opening through multiple layers, such as the contact hole 32, is not a via.

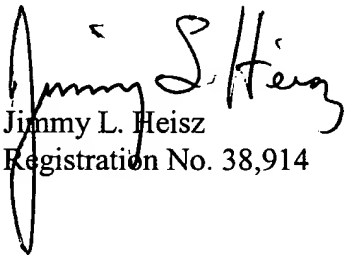
Moreover, those skilled in the art will recognize that Inohara discloses forming a via by forming the contact hole 32 and subsequently filling the hole 32 with a conductive layer 16a and a conductive member 16b. In addition, the Examiner asserts that the conductor member 16b reads on the second metal feature recited in Claim 29 of the present application. However, the Examiner cannot assert that the single via, comprising the contact hole 32 filled with the conductive layer 16a and conductor member 16b, reads on both the unsegmented via and the second metal feature recited in Claim 29. Thus, Inohara fails to disclose either an unsegmented via or a second metal feature as recited in Claim 29. Because those skilled in the art will recognize that the contact hole 32 filled with the conductive layer 16a and conductor member 16b is a via, Inohara fails to disclose a second metal feature as recited in Claim 29.

Inohara fails to disclose each and every element recited in Claim 29 of the present application and, therefore, fails to anticipate Claim 29 and its dependent Claim 30. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 29 and 30 as anticipated by Inohara.

For all of the foregoing reasons, the Appellant respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's Final Rejections with respect to Claims 21, 24, 25, 29, and 30.

Respectfully submitted,

Hitt Gaines, P.C.



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X. APPENDIX A - CLAIMS

Claims 1-20, 22-23, and 26-28 were previously withdrawn or canceled. The Claims involved in this appeal are as follows:

21. A semiconductor device, comprising:

a first interconnect metal located on or in a first interlevel dielectric layer;

a second interconnect metal located on or in a second interlevel dielectric layer, the second interlevel dielectric layer located over the first interlevel dielectric layer;

a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over the second dielectric layer; and

a via located through the second and third interlevel dielectric layers and connecting the first and third interconnect metals, the via being void of a landing pad between the second and third interlevel dielectric layers.

24. The semiconductor device as recited in Claim 21 wherein the via is a passing metal via with no passing metal feature.

25. The semiconductor device as recited in Claim 21 further including transistors wherein the first metal feature is located over the transistors and interconnects the transistors to form an operative integrated circuit.

29. A semiconductor device, comprising:

a first metal feature located on a semiconductor surface;

a first etch stop layer located on the first metal feature;

a first interlevel dielectric layer located on the first etch stop layer;

a second etch stop layer located on the first interlevel dielectric layer;

a second interlevel dielectric layer located on the second etch stop layer;

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the unsegmented via extending to and contacting the first metal feature and being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

30. The semiconductor device as recited in Claim 29 wherein the unsegmented via is a passing metal via with no passing metal feature.

APPENDIX B

FIG. 8